2185

PATENT
5732-00300/MA-069

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Verma et al.

Serial No. 10/080,036

Filed: February 19, 2002

For: MEMORY MODULE HAVING INTERCONNECTED AND STACKED INTEGRATED CIRCUITS

Group Art Unit: 2185
Examiner: Unknown

Atty. Dkt. No. 5732-00300

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on the date indicated below:

5/9/02
Date

Kevin L. Daffer

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Applicant requests consideration of ☒ the references listed on the attached Form PTO-1449 and/or ☐ the additional information identified below in paragraph 3. A copy of each reference listed on the Form PTO-1449 is enclosed.

1. This Information Disclosure Statement is submitted:

a. ☐ within 3 months of the filing date of a national application other than a continued prosecution application under § 1.53(d);
☐ within 3 months of the date of entry of the national stage as set forth in § 1.491 in an International application;
☒ before the mailing date of a first Office Action on the merits; or
☐ before the mailing of a first Office Action after the filing of a request for continued examination under § 1.114.

b. ☐ after the events of above paragraph 1a and prior to the mailing date of a final Office Action or Notice of Allowance, and thus: ☐ the certification of paragraph 2 below is provided, or ☐ a fee of $180.00 is enclosed.

c. ☐ after the mailing date of a final Office Action or a Notice of Allowance and prior to payment of the issue fee, and thus: the certification of paragraph 2 below is provided and a fee of $180.00 is enclosed.

2. It is hereby certified:

☐ that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the Statement, or

☐ that no item of information contained in the Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the person signing the certification after making reasonable inquiry, was known to any individual designated in § 1.56 (c) more than three months prior to the filing of the Statement.

3. ☐ Consideration of the following additional information (including any co-pending or abandoned U.S. applications, prior uses and/or sales, etc.) is requested:

4. For each non-English language reference listed on the attached Form PTO-1449:

☐ reference is made to an English language translation submitted herewith, and/or

☐ reference is made to a foreign patent office search report (in the English language) submitted herewith, and/or

☐ reference is made to an English language translation of a foreign patent office search report submitted herewith, and/or

☐ reference is made to the concise explanation contained in the specification of the present application at page(s) _____, and/or

☐ reference is made to the concise explanation set forth below:

5. ☐ Applicant also offers the following comments for the Examiner's consideration:

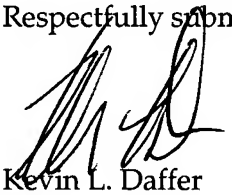
6. ☐ Also enclosed is a copy of a foreign search report citing these references.

7. ☐ The listed documents were brought to the attention of the Applicant(s) after payment of the issue fee in the captioned case. The documents were cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. Applicant(s) request this Information Disclosure Statement and attached Form PTO-1449 be placed in the file of the captioned application.

8. ☐ Applicant(s) requests that the Information Disclosure Statement and attached Form PTO-1449 and references, which are being filed before the grant of the patent and pursuant to 37 C.F.R. § 1.97(i), be placed in the file of the captioned application.

If any required fees are missing, the Commissioner is authorized to charge said fees to Conley, Rose & Tayon, P.C. Deposit Account No. 50-1505/5732-00300.

Respectfully submitted,



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(512) 476-1400

Date: 5/9/02

Form PTO-1449 (modified) List of Patents and Publications For Applicant's Information Disclosure Statement (Use several sheets if necessary)	ATTY. DKT. NO. 5732-00100 APPLICANT: Chhor et al. FILING DATE: August 13, 2001	SERIAL NO. 09/928,767 GROUP: 2818

U.S. PATENT DOCUMENTS

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	A1	3,414,892	12/1968	McCormack et al.			
	A2	3,432,827	3/1969	Sarno			
	A3	4,489,478	12/1984	Sakurai			
	A4	4,500,905	2/1985	Shibata			
	A5	4,535,424	8/1985	Reid			
	A6	4,630,096	12/1986	Drye et al.			
	A7	4,672,577	6/1987	Hirose et al.			
	A8	4,710,798	12/1987	Marcantonio			
	A9	4,811,082	3/1989	Jacobs et al.			
	A10	5,001,539	3/1991	Inoue et al.			
	A11	5,089,862	2/1992	Warner, Jr. et al.			
	A12	5,160,987	11/1992	Pricer et al.			
	A13	5,191,405	3/1993	Tomita et al.			
	A14	5,202,754	4/1993	Bertin et al.			
	A15	5,227,338	7/1993	Kryzaniwsky			
	A16	5,266,912	11/1993	Kledzik			
	A17	5,283,468	2/1994	Kondo et al.			
	A18	5,398,200	3/1995	Mazuré et al.			
	A19	5,422,435	6/1995	Takiar et al.			
	A20	5,426,566	6/1995	Beilstein, Jr. et al.			
	A21	5,434,745	7/1995	Shokrgozar et al.			
	A22	5,453,952	9/1995	Okudaira et al.			
	A23	5,455,445	10/1995	Kurtz et al.			
	A24	5,468,997	11/1995	Imai et al.			
	A25	5,481,090	1/1996	Senock et al.			
	A26	5,481,133	1/1996	Hsu			
	A27	5,495,398	2/1996	Takiar et al.			

EXAMINER: DATE CONSIDERED:

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the patent owner.

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	A28	5,502,289	3/1996	Takiar et al.			
	A29	5,523,622	6/1996	Harada et al.			
	A30	5,523,628	6/1996	Williams et al.			
	A31	5,552,963	9/1996	Burns			
	A32	5,561,622	10/1996	Bertin et al.			
	A33	5,581,498	12/1996	Ludwig et al.			
	A34	5,585,675	12/1996	Knopf			
	A35	5,612,570	3/1997	Eide et al.			
	A36	5,654,220	8/1997	Leedy			
	A37	5,693,552	12/1997	Hsu			
	A38	5,696,031	12/1997	Wark			
	A39	5,702,985	12/1997	Burns			
	A40	5,703,747	12/1997	Voldman et al.			
	A41	5,780,925	7/1998	Cipolla et al.			
	A42	5,781,031	7/1998	Bertin et al.			
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	A44	5,801,437	9/1998	Burns			
	A45	5,915,167	6/1999	Leedy			
	A46	5,969,380	10/1999	Seyyedy			
	A47	5,973,951	10/1999	Bechtolsheim et al.			
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	A50	6,057,598	5/2000	Payne et al.			
	A51	6,072,234	6/2000	Camien et al.			
	A52	6,085,412	7/2000	Iwasaki			
	A53	6,087,722	7/2000	Lee et al.			
	A54	6,108,730	8/2000	Dell et al.			

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	A55	6,133,640	10/2000	Leedy			
	A56	6,185,122	2/2001	Johnson et al.			
	A57	6,197,641	3/2001	Hergenrother et al.			
	A58	6,208,545	3/2001	Leedy			
	A59	6,252,791	6/2001	Wallace et al.			
	A60	6,281,042	8/2001	Ahn et al.			
	A61	6,291,858	9/2001	Ma et al.			
	A62	6,307,257	10/2001	Huang et al.			
	A63	6,314,013	11/2001	Ahn et al.			
	A64	6,322,903	11/2001	Siniaguine et al.			
	A65	6,337,521	1/2002	Masuda			
	A66	6,351,028	2/2002	Akram			
	A67	6,353,265	3/2002	Michii			
	A68	6,355,501	3/2002	Fung et al.			

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EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	A69	2001/0033030	10/2001	Leedy			
	A70	2001/0054759	12/2001	Nishiura			
	A71	2002/0024146	2/2002	Furusawa			
	A72	2002/0027275	3/2002	Fujimoto et al.			
	A73	2002/0030262	3/2002	Akram			
	A74	2002/0030263	3/2002	Akram			

FOREIGN PATENT DOCUMENTS

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
	A75	0 073 486	3/1983	EP			
	A76	0 387 834	9/1990	EP			

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	A77	0 395 886	11/1990	EP			
	A78	0 516 866	12/1992	EP			Yes, Abstract Only
	A79	0 606 653	7/1994	EP			
	A80	0 644 548	3/1995	EP			
	A81	0 800 137	10/1997	EP			
	A82	60-22352	2/1985	JP			Yes, Abstract Only
	A83	61-222216	10/1986	JP			Yes, Abstract Only
	A84	63-52463	3/1988	JP			Yes, Abstract Only
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	A86	Akasaka, "Three-dimensional integrated circuit: technology and application prospect," Microelectronics Journal, Vol. 20, Nos. 1-2, 1989, pp. 105-112.
	A87	Sakamoto, "Architecture des Circuits à Trois Dimensions," Bulletin of the Electrotechnical Laboratory, Vol. 51, No. 1, 1987, pp. 16-29.
	A88	Akasaka, "Three-Dimensional IC Trends," Proceedings of the IEEE, Vol. 74, No. 12, 1986, pp. 1703-1714.
	A89	Pein et al., "Performance of the 3-D PENCIL Flash EPROM Cell and Memory Array," IEEE Transactions on Electron Devices, Vol. 42, No. 11, 1995, pp. 1982-1991.
	A90	Jokerst et al., "Manufacturable Multi-Material Integration: Compound Semiconductor Devices Bonded to Silicon Circuitry," SPIE Vol. 2524, 1995, pp. 152-163.
	A91	Camperi-Ginestet et al., "Vertical Electrical Interconnection of Compound Semiconductor Thin-Film Devices to Underlying Silicon Circuitry," IEEE Photonics Technology Letters, Vol. 4, No. 9, 1992, pp. 1003-1006.
	A92	Lomatch et al., "Multilayered Josephson junction logic and memory devices," SPIE Vol. 2157, 1994, Abstract Only, 2 pgs.
	A93	Lu, "Advanced cell structures for dynamic RAMs," IEEE Circuits and Devices, Vol. 5, No. 1, 1989, Abstract Only, 2 pgs.
	A94	Sakamoto, "Architecture of three dimensional devices," Bulletin of the Electrotechnical Laboratory, Vol. 51, No. 1, 1987, Abstract Only, 2 pgs.

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		OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)
	A95	"Wide application of low-cost associative processing seen," Electronic Engineering Times, 1996, 6 pgs.
	A96	"Interconnects & Packaging," Electronic Engineering Times, 1996, 8 pgs.
	A97	"Closing in on gigabit DRAMs," Electronic Engineering Times, 1995, 4 pgs.
	A98	"Module Pact Pairs Cubic Memory with VisionTek," Semiconductor Industry & Business Survey, Vol. 17, No. 15, 1995, 2 pgs.
	A99	Flaherty, "Layers of BST materials push toward 1Gbit DRAM," Electronic Times, 1995, 3 pgs.
	A100	Santoni, "Technologies Will Pursue Higher DRAM Densities," Electronic News, 1991, 7 pgs.
	A101	Weber, "Looking for diverse storage," Electronic Engineering Times, 1994, 7 pgs.
	A102	"Special Report: Memory Market Startups, Cubic Memory: 3D Space Savers," Semiconductor Industry & Business Survey, Vol. 16, No. 13, 1994, 6 pgs.
	A103	Bindra, "Technique boosts 3D memory density," Electronic Engineering Times, 1994, 2 pgs.
	A104	Bindra, "Memory packs poised for 3-D use," Electronic Engineering Times, 1992, 4 pgs.
	A105	Derman, "MCMs hit the road," Electronic Engineering Times, 1992, 6 pgs.
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	A107	"Tech Watch: 1-Gbit DRAM in sight," Electronic World News, 1991, 2 pgs.
	A108	Derman, "MCMs meld into systems," Electronic Engineering Times, 1991, 7 pgs.
	A109	Brown, "Systems EEs see future in 3-D," Electronic Engineering Times, 1990, 4 pgs.
	A110	Hayashi et al., "A New Three Dimensional IC Fabrication Technology, Stacking Thin Film Dual CMOS Layers," © 1991 IEEE, 4 pgs.
	A111	Tielert, "Benefits of Vertically Stacked Integrated Circuits for Sequential Logic," © 1996 IEEE, pp. 121-124.
	A112	Stern et al., "Design and Evaluation of an Epoxy Three-Dimensional Multichip Module," IEEE Transactions on Components, Packaging, and Manufacturing Technology - Part B, Vol. 19, No. 1, 1996, pp. 188-194.
	A113	Bertin et al., "Evaluation of a Three-Dimensional Memory Cube System," IEEE Transactions on Components, Hybrids, and Manufacturing Technology, Vol. 16, No. 8, 1993, pp. 1006-1011.
	A114	Watanabe et al., "Stacked Capacitor Cells for High-density dynamic RAMs," © 1988 IEEE, pp. 600-604.
	A115	"Stacked Memory Modules," IBM Technical Disclosure Bulletin, Vol. 38, No. 5, 1995, 2 pgs.
	A116	"3-D Chip-on-chip Stacking," Semiconductor International, 1991, 1 pg.
	A117	Thakur et al., "An Optimal Layer Assignment Algorithm for Minimizing Crosstalk for Three Layer VHV Channel Routing," © 1995 IEEE, pp. 207-210.

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OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)		
	A118	Terrill et al., "3D Packaging Technology Overview and Mass Memory Applications," © 1996 IEEE, pp. 347-355.
	A119	Sugahara et al., "A Three-Dimensional Static RAM," IEEE Electron Device Letters, Vol. EDL7, No. 5, 1986, pp. 327-329.
	A120	Tielert, "Benefits of Vertically Stacked Integrated Circuits for Sequential Logic," © 1996 IEEE, pp. 121-124.
	A121	Akasaka, "Three-Dimensional IC Trends," © 1986 IEEE, pp. 1703-1714.
	A122	Kurokawa et al., "3-D VLSI Technology in Japan and an Example: a Syndrome Decoder for Double Error Correction," Future Generation Computer Systems, Vol. 4, No. 2, 1988, pp. 145-155.
	A123	Maliniak, "Memory-Chip Stacks Send Density Skyward," Electronic Design, Vol. 42, No. 17, 1994, 5 pgs.
	A124	Schlaeppi et al., "Submicrosecond Core Memories Using Multiple Coincidence," IRE Transactions on Electronic Computers, 1960, pp. 192-198.
	A125	Schlaeppi et al., "Submicrosecond Core Memories Using Multiple Coincidence," 1960 International Solid State Circuits Conference, pp. 54-55.
	A126	Lay, "TRW Develops Wireless Multiboard Interconnect System," Electronic Engineering Times, 1984, 1 pg.
	A127	Yamazaki et al., "Fabrication Technologies for Dual 4-Kbit Stacked SRAM," © 1986 IEEE, pp. 435-438.
	A128	Dipert, "Exotic memories, diverse approaches," EDN Asia, September 2001, pp. 22-33.

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